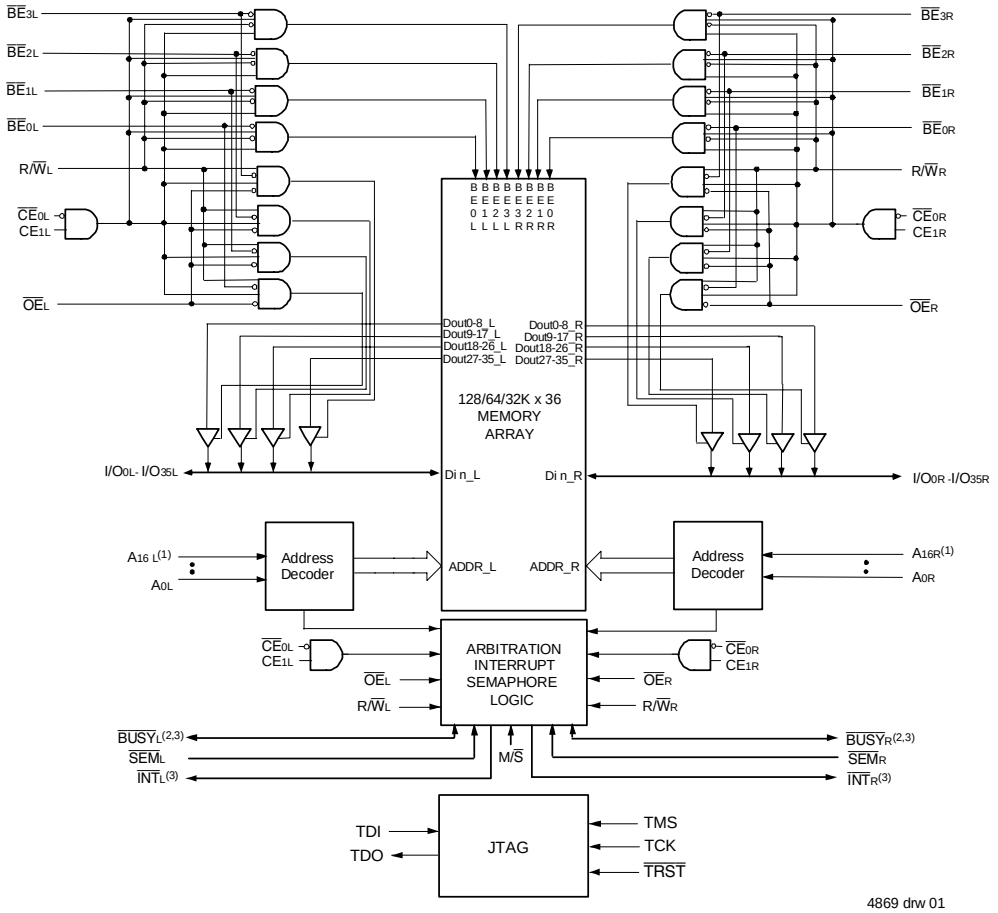
HIGH-SPEED 3.3V 128/64/32K x 36 ASYNCHRONOUS DUAL-PORT STATIC RAM

IDT70V659/58/57S

Features

- True Dual-Port memory cells which allow simultaneous access of the same memory location
- High-speed access
  - *Commercial: 10/12/15ns (max.)*
  - *Industrial: 12/15ns (max.)*
- Dual chip enables allow for depth expansion without external logic
- IDT70V659/58/57 easily expands data bus width to 72 bits or more using the Master/Slave select when cascading more than one device
- M/$\overline{S}$ = VIH for $\overline{BUSY}$ output flag on Master, M/$\overline{S}$ = VIL for $\overline{BUSY}$ input on Slave
- Busy and Interrupt Flags
- On-chip port arbitration logic
- Full on-chip hardware support of semaphore signaling between ports
- Fully asynchronous operation from either port
- Separate byte controls for multiplexed bus and bus matching compatibility
- Supports JTAG features compliant to IEEE 1149.1
- LVTTL-compatible, single 3.3V (±150mV) power supply for core
- LVTTL-compatible, selectable 3.3V (±150mV)/2.5V (±100mV) power supply for I/Os and control signals on each port
- Available in a 208-pin Plastic Quad Flatpack, 208-ball fine pitch Ball Grid Array, and 256-ball Ball Grid Array
- Industrial temperature range (–40°C to +85°C) is available for selected speeds
- Green parts available, see ordering information

Functional Block Diagram



4869 drw 01

NOTES:

1. A16 is a NC for IDT70V658. Also, Addresses A16 and A15 are NC's for IDT70V657.
2. $\overline{BUSY}$ is an input as a Slave (M/$\overline{S}$=VIL) and an output when it is a Master (M/$\overline{S}$=VIH).
3. $\overline{BUSY}$ and $\overline{INT}$ are non-tri-state totem-pole outputs (push-pull).

Description

The IDT70V659/58/57 is a high-speed 128/64/32K x 36 Asynchronous Dual-Port Static RAM. The IDT70V659/58/57 is designed to be used as a stand-alone 4/2/1Mbit Dual-Port RAM or as a combination MASTER/SLAVE Dual-Port RAM for 72-bit-or-more word system. Using the IDT MASTER/SLAVE Dual-Port RAM approach in 72-bit or wider memory system applications results in full-speed, error-free operation without the need for additional discrete logic.

This device provides two independent ports with separate control, address, and I/O pins that permit independent, asynchronous access for reads or writes to any location in memory. An automatic power down feature controlled by the chip enables (either $\overline{CE}_0$ or CE_1) permit the on-chip circuitry of each port to enter a very low standby power mode.

The 70V659/58/57 can support an operating voltage of either 3.3V or 2.5V on one or both ports, controlled by the OPT pins. The power supply for the core of the device (V_{DD}) remains at 3.3V.

Recommended DC Operating Conditions with V_{DDQ} at 2.5V

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{DD}	Core Supply Voltage	3.15	3.3	3.45	V
V_{DDQ}	I/O Supply Voltage[3]	2.4	2.5	2.6	V
V_{SS}	Ground	0	0	0	V
V_{IH}	Input High Voltage[3] (Address & Control Inputs)	1.7	—	V_{DDQ} + 100mV[2]	V
V_{IH}	Input High Voltage - I/O[3]	1.7	—	V_{DDQ} + 100mV[2]	V
V_{IL}	Input Low Voltage	-0.5[1]	—	0.7	V

4869 tbl 06

NOTES:
1. $V_{IL} \geq$ -1.5V for pulse width less than 10 ns.
2. V_{TERM} must not exceed V_{DDQ} + 100mV.
3. To select operation at 2.5V levels on the I/Os and controls of a given port, the OPT pin for that port must be set to V_{SS} (0V), and V_{DDQX} for that port must be supplied as indicated above.

Recommended DC Operating Conditions with V_{DDQ} at 3.3V

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{DD}	Core Supply Voltage	3.15	3.3	3.45	V
V_{DDQ}	I/O Supply Voltage[3]	3.15	3.3	3.45	V
V_{SS}	Ground	0	0	0	V
V_{IH}	Input High Voltage (Address & Control Inputs)[3]	2.0	—	V_{DDQ} + 150mV[2]	V
V_{IH}	Input High Voltage - I/O[3]	2.0	—	V_{DDQ} + 150mV[2]	V
V_{IL}	Input Low Voltage	-0.3[1]	—	0.8	V

4869 tbl 07

NOTES:
1. $V_{IL} \geq$ -1.5V for pulse width less than 10 ns.
2. V_{TERM} must not exceed V_{DDQ} + 150mV.
3. To select operation at 3.3V levels on the I/Os and controls of a given port, the OPT pin for that port must be set to V_{DD} (3.3V), and V_{DDQX} for that port must be supplied as indicated above.

Capacitance[1]

(T_A = +25°C, F = 1.0MHz) PQFP ONLY

Symbol	Parameter	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	8	pF
C_{OUT}[2]	Output Capacitance	V_{OUT} = 0V	10.5	pF

4869 tbl 08

NOTES:
1. These parameters are determined by device characterization, but are not production tested.
2. C_{OUT} also references $C_{I/O}$.

Maximum Operating Temperature and Supply Voltage[1]

Grade	Ambient Temperature	GND	V_{DD}
Commercial	0°C to +70°C	0V	3.3V ± 150mV
Industrial	-40°C to +85°C	0V	3.3V ± 150mV

4869 tbl 04

NOTE:
1. This is the parameter TA. This is the "instant on" case temperature.

Absolute Maximum Ratings[1]

Symbol	Rating	Commercial & Industrial	Unit
V_{TERM}[2] (V_{DD})	V_{DD} Terminal Voltage with Respect to GND	-0.5 to + 4.6	V
T_{BIAS}[3]	Temperature Under Bias	-55 to +125	°C
T_{STG}	Storage Temperature	-65 to +150	°C
T_{JN}	Junction Temperature	+150	°C
I_{OUT}(For V_{DDQ} = 3.3V)	DC Output Current	50	mA
I_{OUT}(For V_{DDQ} = 2.5V)	DC Output Current	40	mA

4869 tbl 05

NOTES:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. V_{TERM} must not exceed V_{DD} + 150mV for more than 25% of the cycle time or 4ns maximum, and is limited to $\leq$ 20mA for the period of $V_{TERM} \geq V_{DD}$ + 150mV.
3. Ambient Temperature under DC Bias. No AC Conditions. Chip Deselected.

DC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range (V_{DD} = 3.3V ± 150mV)

Symbol	Parameter	Test Conditions	70V659/58/57S Min.	70V659/58/57S Max.	Unit
$\|I_{LI}\|$	Input Leakage Current[1]	V_{DDQ} = Max., V_{IN} = 0V to V_{DDQ}	—	10	µA
$\|I_{LO}\|$	Output Leakage Current	$\overline{CE}_0$ = V_{IH} or CE_1 = V_{IL}, V_{OUT} = 0V to V_{DDQ}	—	10	µA
V_{OL} (3.3V)	Output Low Voltage[2]	I_{OL} = +4mA, V_{DDQ} = Min.	—	0.4	V
V_{OH} (3.3V)	Output High Voltage[2]	I_{OH} = -4mA, V_{DDQ} = Min.	2.4	—	V
V_{OL} (2.5V)	Output Low Voltage[2]	I_{OL} = +2mA, V_{DDQ} = Min.	—	0.4	V
V_{OH} (2.5V)	Output High Voltage[2]	I_{OH} = -2mA, V_{DDQ} = Min.	2.0	—	V

4869 tbl 09

NOTE:
1. At V_{DD} ≤ - 2.0V input leakages are undefined.
2. V_{DDQ} is selectable (3.3V/2.5V) via OPT pins. Refer to p.6 for details.

DC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range[3] (V_{DD} = 3.3V ± 150mV)

Symbol	Parameter	Test Condition	Version	70V659/58/57S10 Com'l Only Typ.[4]	70V659/58/57S10 Com'l Only Max.	70V659/58/57S12 Com'l & Ind Typ.[4]	70V659/58/57S12 Com'l & Ind Max.	70V659/58/57S15 Com'l & Ind Typ.[4]	70V659/58/57S15 Com'l & Ind Max.	Unit
I_{DD}	Dynamic Operating Current (Both Ports Active)	$\overline{CE}_L$ and $\overline{CE}_R$ = V_{IL}, Outputs Disabled, f = f_{MAX}[1]	COM'L S	340	500	315	465	300	440	mA
			IND S	—	—	365	515	350	490	
I_{SB1}	Standby Current (Both Ports - TTL Level Inputs)	$\overline{CE}_L$ = $\overline{CE}_R$ = V_{IH}, f = f_{MAX}[1]	COM'L S	115	165	90	125	75	100	mA
			IND S	—	—	115	150	100	125	
I_{SB2}	Standby Current (One Port - TTL Level Inputs)	$\overline{CE}_{"A"}$ = V_{IL} and $\overline{CE}_{"B"}$ = V_{IH}[5] Active Port Outputs Disabled, f=f_{MAX}[1]	COM'L S	225	340	200	325	175	315	mA
			IND S	—	—	225	365	200	350	
I_{SB3}	Full Standby Current (Both Ports - CMOS Level Inputs)	Both Ports $\overline{CE}_L$ and $\overline{CE}_R$ ≥ V_{DDQ} - 0.2V, V_{IN} ≥ V_{DDQ} - 0.2V or V_{IN} ≤ 0.2V, f = 0[2]	COM'L S	3	15	3	15	3	15	mA
			IND S	—	—	6	15	6	15	
I_{SB4}	Full Standby Current (One Port - CMOS Level Inputs)	$\overline{CE}_{"A"}$ ≤ 0.2V and $\overline{CE}_{"B"}$ ≥ V_{DDQ} - 0.2V[5] V_{IN} ≥ V_{DDQ} - 0.2V or V_{IN} ≤ 0.2V, Active Port, Outputs Disabled, f = f_{MAX}[1]	COM'L S	220	335	195	320	170	310	mA
			IND S	—	—	220	360	195	345	

4869 tbl 10

NOTES:
1. At f = f_{MAX}, address and control lines (except Output Enable) are cycling at the maximum frequency read cycle of 1/t_{RC}, using "AC TEST CONDITIONS" at input levels of GND to 3V.
2. f = 0 means no address or control lines change. Applies only to input at CMOS level standby.
3. Port "A" may be either left or right port. Port "B" is the opposite from port "A".
4. V_{DD} = 3.3V, T_A = 25°C for Typ, and are not production tested. $I_{DD\,DC}$(f=0) = 120mA (Typ).
5. $\overline{CE}_X$ = V_{IL} means $\overline{CE}_{0X}$ = V_{IL} and CE_{1X} = V_{IH}
   $\overline{CE}_X$ = V_{IH} means $\overline{CE}_{0X}$ = V_{IH} or CE_{1X} = V_{IL}
   $\overline{CE}_X$ ≤ 0.2V means $\overline{CE}_{0X}$ ≤ 0.2V and CE_{1X} ≥ V_{DDQ} - 0.2V
   $\overline{CE}_X$ ≥ V_{DDQ} - 0.2V means $\overline{CE}_{0X}$ ≥ V_{DDQ} - 0.2V or CE_{1X} - 0.2V
   "X" represents "L" for left port or "R" for right port.

AC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range(5)

Symbol	Parameter	70V659/58/57S10 Com'l Only		70V659/58/57S12 Com'l & Ind		70V659/58/57S15 Com'l & Ind		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE								
t_{RC}	Read Cycle Time	10	—	12	—	15	—	ns
t_{AA}	Address Access Time	—	10	—	12	—	15	ns
t_{ACE}	Chip Enable Access Time(3)	—	10	—	12	—	15	ns
t_{ABE}	Byte Enable Access Time(3)	—	5	—	6	—	7	ns
t_{AOE}	Output Enable Access Time	—	5	—	6	—	7	ns
t_{OH}	Output Hold from Address Change	3	—	3	—	3	—	ns
t_{LZ}	Output Low-Z Time(1,2)	0	—	0	—	0	—	ns
t_{HZ}	Output High-Z Time(1,2)	0	4	0	6	0	8	ns
t_{PU}	Chip Enable to Power Up Time(2)	0	—	0	—	0	—	ns
t_{PD}	Chip Disable to Power Down Time(2)	—	10	—	10	—	15	ns
t_{SOP}	Semaphore Flag Update Pulse ($\overline{OE}$ or $\overline{SEM}$)	—	4	—	6	—	8	ns
t_{SAA}	Semaphore Address Access Time	3	10	3	12	3	20	ns

4869 tbl 12

AC Electrical Characteristics Over the Operating Temperature and Supply Voltage(5)

Symbol	Parameter	70V659/58/57S10 Com'l Only		70V659/58/57S12 Com'l & Ind		70V659/58/57S15 Com'l & Ind		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
WRITE CYCLE								
t_{WC}	Write Cycle Time	10	—	12	—	15	—	ns
t_{EW}	Chip Enable to End-of-Write(3)	8	—	10	—	12	—	ns
t_{AW}	Address Valid to End-of-Write	8	—	10	—	12	—	ns
t_{AS}	Address Set-up Time(3)	0	—	0	—	0	—	ns
t_{WP}	Write Pulse Width	8	—	10	—	12	—	ns
t_{WR}	Write Recovery Time	0	—	0	—	0	—	ns
t_{DW}	Data Valid to End-of-Write	6	—	8	—	10	—	ns
t_{DH}	Data Hold Time(4)	0	—	0	—	0	—	ns
t_{WZ}	Write Enable to Output in High-Z(1,2)	—	4	—	4	—	4	ns
t_{OW}	Output Active from End-of-Write(1,2,4)	0	—	0	—	0	—	ns
t_{SWRD}	$\overline{SEM}$ Flag Write to Read Time	5	—	5	—	5	—	ns
t_{SPS}	$\overline{SEM}$ Flag Contention Window	5	—	5	—	5	—	ns

4869 tbl 13

NOTES:
1. Transition is measured 0mV from Low or High-impedance voltage with Output Test Load (Figure 2).
2. This parameter is guaranted by device characterization, but is not production tested.
3. To access RAM, $\overline{CE}$= V_{IL} and $\overline{SEM}$ = V_{IH}. To access semaphore, $\overline{CE}$ = V_{IH} and $\overline{SEM}$ = V_{IL}. Either condition must be valid for the entire t_{EW} time.
4. The specification for t_{DH} must be met by the device supplying write data to the RAM under all operating conditions. Although t_{DH} and t_{OW} values will vary over voltage and temperature, the actual t_{DH} will always be smaller than the actual t_{OW}.
5. These values are valid regardless of the power supply level selected for I/O and control signals (3.3V/2.5V). See page 6 for details.

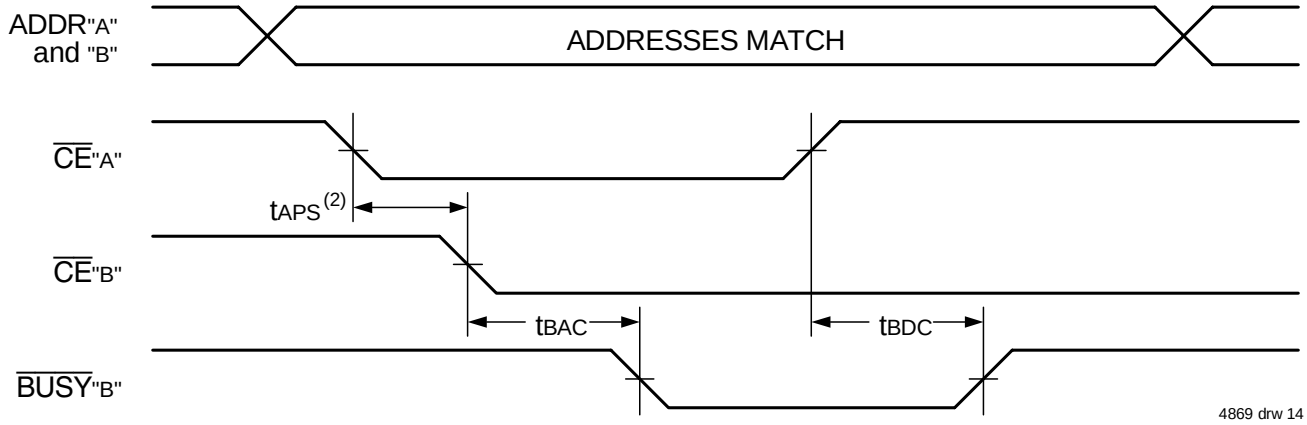
AC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range

Symbol	Parameter	70V659/58/57S10 Com'l Only		70V659/58/57S12 Com'l & Ind		70V659/58/57S15 Com'l & Ind		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
$\overline{BUSY}$ TIMING (M/$\overline{S}$=VIH)								
t_{BAA}	$\overline{BUSY}$ Access Time from Address Match	—	10	—	12	—	15	ns
t_{BDA}	$\overline{BUSY}$ Disable Time from Address Not Matched	—	10	—	12	—	15	ns
t_{BAC}	$\overline{BUSY}$ Access Time from Chip Enable Low	—	10	—	12	—	15	ns
t_{BDC}	$\overline{BUSY}$ Disable Time from Chip Enable High	—	10	—	12	—	15	ns
t_{APS}	Arbitration Priority Set-up Time[2]	5	—	5	—	5	—	ns
t_{BDD}	$\overline{BUSY}$ Disable to Valid Data[3]	—	10	—	12	—	15	ns
t_{WH}	Write Hold After $\overline{BUSY}$[5]	8	—	10	—	12	—	ns
$\overline{BUSY}$ TIMING (M/$\overline{S}$=VIL)								
t_{WB}	$\overline{BUSY}$ Input to Write[4]	0	—	0	—	0	—	ns
t_{WH}	Write Hold After $\overline{BUSY}$[5]	8	—	10	—	12	—	ns
PORT-TO-PORT DELAY TIMING								
t_{WDD}	Write Pulse to Data Delay[1]	—	22	—	25	—	30	ns
t_{DDD}	Write Data Valid to Read Data Delay[1]	—	20	—	22	—	25	ns

4869 tbl 14

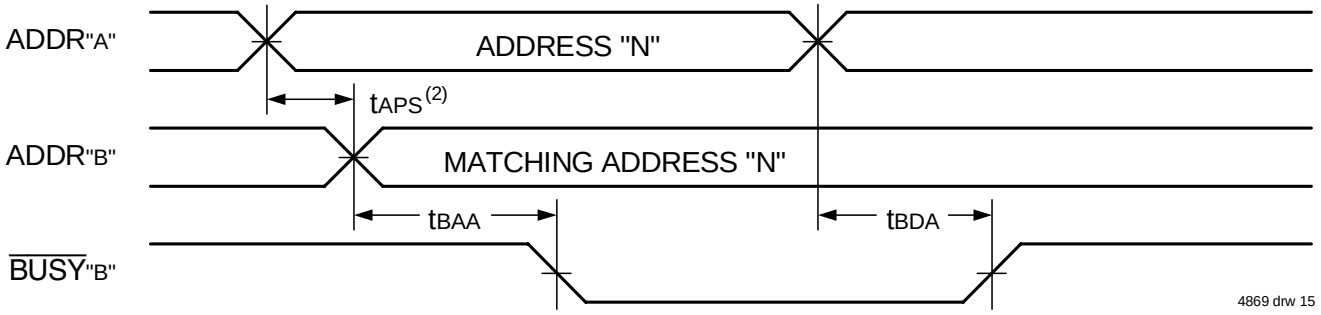
NOTES:
1. Port-to-port delay through RAM cells from writing port to reading port, refer to "Timing Waveform of Write with Port-to-Port Read and $\overline{BUSY}$ (M/$\overline{S}$ = VIH)".
2. To ensure that the earlier of the two ports wins.
3. t_{BDD} is a calculated parameter and is the greater of the Max. spec, t_{WDD} – t_{WP} (actual), or t_{DDD} – t_{DW} (actual).
4. To ensure that the write cycle is inhibited on port "B" during contention on port "A".
5. To ensure that a write cycle is completed on port "B" after contention on port "A".

Waveform of $\overline{BUSY}$ Arbitration Controlled by $\overline{CE}$ Timing (M/$\overline{S}$ = VIH)(1)



4869 drw 14

Waveform of $\overline{BUSY}$ Arbitration Cycle Controlled by Address Match Timing (M/$\overline{S}$ = VIH)(1)



4869 drw 15

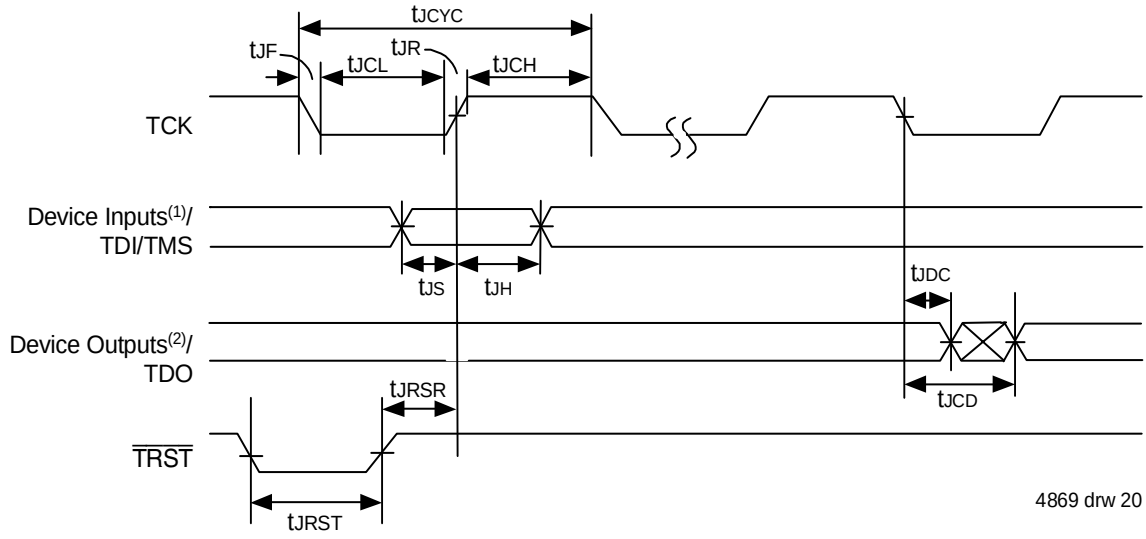
NOTES:
1. All timing is the same for left and right ports. Port "A" may be either the left or right port. Port "B" is the port opposite from port "A".
2. If tAPS is not satisfied, the $\overline{BUSY}$ signal will be asserted on one side or another but there is no guarantee on which side $\overline{BUSY}$ will be asserted.

AC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range

		70V659/58/57S10 Com'l Only		70V659/58/57S12 Com'l & Ind		70V659/58/57S15 Com'l & Ind		
Symbol	**Parameter**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Unit**
INTERRUPT TIMING								
tAS	Address Set-up Time	0	—	0	—	0	—	ns
tWR	Write Recovery Time	0	—	0	—	0	—	ns
tINS	Interrupt Set Time	—	10	—	12	—	15	ns
tINR	Interrupt Reset Time	—	10	—	12	—	15	ns

4869 tbl 15

JTAG Timing Specifications



NOTES:
1. Device inputs = All device inputs except TDI, TMS, and TRST.
2. Device outputs = All device outputs except TDO.

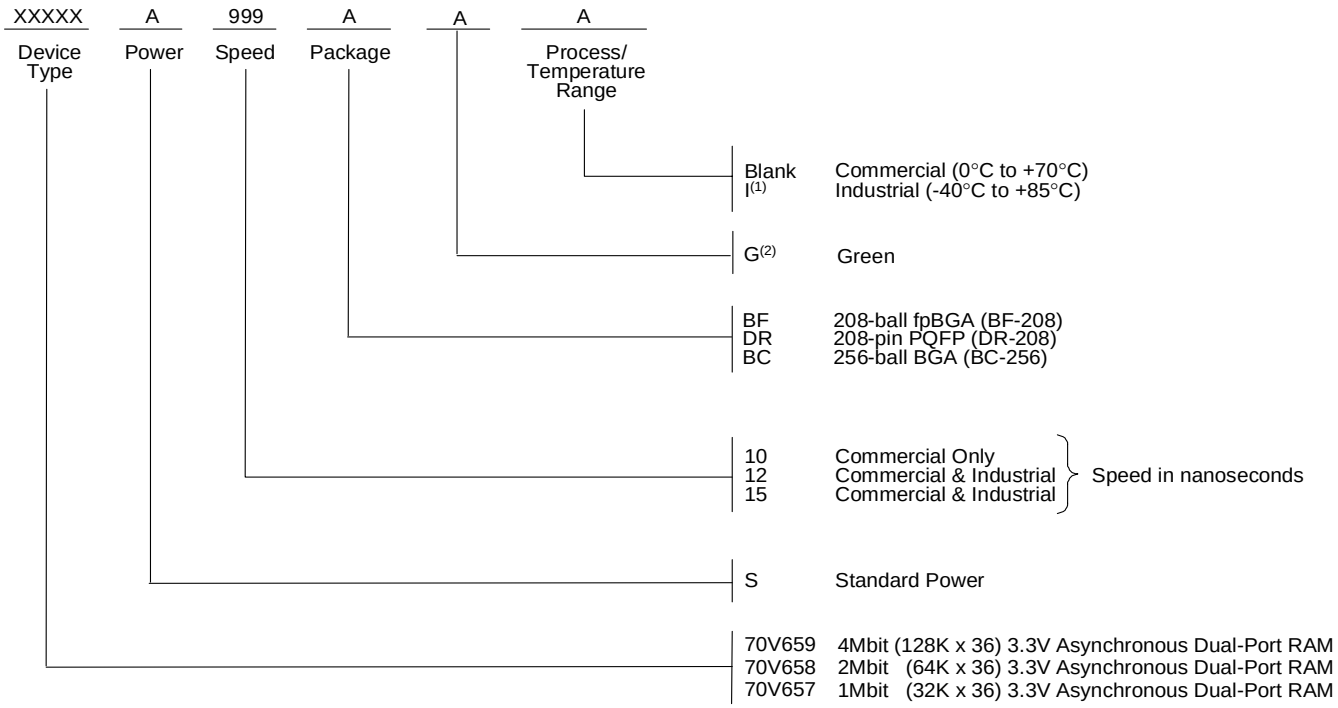
JTAG AC Electrical Characteristics(1,2,3,4)

Symbol	Parameter	Min.	Max.	Units
tJCYC	JTAG Clock Input Period	100	—	ns
tJCH	JTAG Clock HIGH	40	—	ns
tJCL	JTAG Clock Low	40	—	ns
tJR	JTAG Clock Rise Time	—	3(1)	ns
tJF	JTAG Clock Fall Time	—	3(1)	ns
tJRST	JTAG Reset	50	—	ns
tJRSR	JTAG Reset Recovery	50	—	ns
tJCD	JTAG Data Output	—	25	ns
tJDC	JTAG Data Output Hold	0	—	ns
tJS	JTAG Setup	15	—	ns
tJH	JTAG Hold	15	—	ns

4869 tbl 19

NOTES:
1. Guaranteed by design.
2. 30pF loading on external output signals.
3. Refer to AC Electrical Test Conditions stated earlier in this document.
4. JTAG operations occur at one speed (10MHz). The base device may run at any speed specified in this datasheet.

Ordering Information



4869 drw 21

Notes:

1. Contact your local sales office for Industrial temp range in other speeds, packages and powers.
2. Green parts available. For specific speeds, packages and powers contact your local sales office.